1. (Once Amended) A device for data stream analyzing, comprising a processor means and a program memory making it possible to parse a data stream in a way that is controlled by an interchangeable program.

2. (Once Amended) A device according to claim 1, further comprising a multiplexable data stream delayline for receiving said data stream, and multiplexing means for connecting different parts of the data stream to said processor means.

3. (Once Amended) A device according to claim 2, wherein the multiplexing means includes a multiplexing control means for automatically keeping track of where specific data is located in the delayline, making it possible to write programs for controlling the device that can start executing at any time after the data have arrived to the device, and without the need for starting execution at a specific time relative to when the data stream was entering the device.

4. (Once Amended) A device according to claim 2, wherein said delayline comprises a 23 shift deep, 1 byte wide shift register.

5. (Once Amended) A device according to claim 3, wherein the multiplexing control means automatically keeps track of where specific data is located in the delayline by the use of a first and second position register that change according to certain

rules when a packet is forwarded in the delayline.

6. (Once Amended) A device according to claim 5, wherein values of the position registers are changed in the following way; when a packet arrives, the first register starts to increment for every byte; when the packet has come to its end where the packets DV (data valid) signal becomes false again, the first register stops counting and the second register starts to increment.

7. (Once Amended) A device according to claim 5, which automatically keeps track of where specific data is located in the delayline, by the use of said dedicated position registers together with the use of a formula

$$P = \text{tagfield} + \text{lastfield} - \text{wanted\_tag}$$

and "P" is the position of a wanted byte in the delayline; "tagfield" is the value of the first register; "lastfield" is the value of the second register and "wanted_tag" is the position of the wanted byte relative to the beginning of the packet.

8. (Once Amended) A device according to claim 1, further comprising a plurality of registers for making logical and/or arithmetic operations on data-stream data, before an actual comparison of the data with other data is executed.

9. (Once Amended) A device according to claim 1, further comprising a stack memory means which enables the

writing of one or more programs with subroutines for reducing the need for large program memories.

10. ~~(Once Amended) A device according to claim 1,~~ further comprising a base address register for the processor means to make it possible to reuse code to recognize a given pattern even it starts at different positions in the data stream.

11. (Once Amended) A device according to claim 1, wherein the program memory is of double ported type.

In the Abstract

Please replace the paragraph on page 11, beginning at line 2, with the following rewritten paragraph.:

A device for data stream analyzing that is able to recognize different data streams and then start processors or functionalities to store or check data in a data stream. The device includes a processor means and a program memory, making it possible to parse a data stream in a way that is controlled by an interchangeable program. There will be no need for changing the hardware. This could save time and money for companies responsible for providing, maintaining and updating network switches. The device also includes a multiplexable data stream delayline for receiving the data streams, and multiplexing means for connecting different parts of the data stream to the processor means.